

CLAIMS

What is claimed is:

1. An application specific integrated circuit (ASIC) comprising:
 - 2 a standard cell, the standard cell including a plurality of logic functions; and
 - 3 at least one FPGA interconnect coupled to the plurality of functions, wherein
 - 4 the at least one FPGA interconnect can be configured to select one of the plurality of logic
 - 5 functions.
2. The ASIC of claim 1 wherein the one logic function is coupled to a plurality of I/O pins by the at least one configured FPGA interconnect.
3. The ASIC of claim 1 wherein the one logic function is coupled to an internal bus via the at least one configured FPGA interconnect.
4. An application specific integrated circuit (ASIC) comprising:
 - 2 a standard cell, the standard cell including a plurality of logic functions;
 - 3 a plurality of input output (I/O) pins; and
 - 4 at least one field programmable gate array (FPGA) interconnect coupled the
 - 5 plurality of I/O pins and the plurality of logic functions, wherein the at least one FPGA
 - 6 interconnect can be configured to select one of the plurality of logic functions utilizing field
 - 7 programming techniques.

1 5. The ASIC of claim 4 wherein the one logic function is coupled to an internal
2 bus via the at least one configured FPGA interconnect.

1 6. An application specific integrated circuit (ASIC) comprising:
2 a standard cell, the standard cell including a plurality of logic functions;
3 a at least one internal bus; and
4 at least one field programmable gate array (FPGA) interconnect coupled to at
5 least one internal bus and the plurality of logic functions, wherein the at least one FPGA
6 interconnect can be configured to select one of the plurality of logic functions utilizing field
7 programming techniques.

1 7. The ASIC of claim 6 wherein the one logic function is coupled to a plurality of
2 I/O pins by the at least one configured FPGA interconnect.

1 8. An application specific integrated circuit (ASIC) comprising:
2 a standard cell, the standard cell including a plurality of logic functions;
3 at least one bus coupled to the plurality of functions;
4 a plurality of I/O pins; and
5 at least one FPGA interconnect coupled between the at least one bus and the
6 plurality of I/O pins, wherein the at least one FPGA interconnect can be utilized to correct
7 wiring error when the ASIC is utilized on a printed circuit board.

1 9. The ASIC of claim 8 wherein the wiring error is a reversed bit order wiring

2 error.

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10. An application specific integrated circuit (ASIC) comprising:
2 a plurality of I/O pins;
3 a plurality of first logic functions;
4 a first field programmable gate array (FPGA) interconnect coupled between the
5 plurality of I/O pins and the plurality of first logic function, wherein the first FPGA
6 interconnect can be configured to select at least one of the plurality of first logic functions;
7 a bus coupled to a plurality of first logic functions; and
8 a second FPGA interconnect coupled between the bus and the plurality of first logic
9 functions, wherein the second FPGA interconnect is configured to connect to one of the
10 plurality of first logic functions to the bus.

11. The ASIC of claim 10 which includes a plurality of second logic functions
12 coupled to the bus.